Q.P. Code: 20CS0503a

R20

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech I Year II Semester Regular & Supplementary Examinations October-2022

DIGITAL LOGIC DESIGN

(Common to CSM, CAD & CIC)

Time: 3 hours | Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	a	Convert the following numbers i)(31.6876)10 to Hexadecimal number ii) (10101101.1001)2 to base-8 and base-4 iii) (3564)10 to base2	L1	6M
	b	Subtract (111001)2 from (101011) using 1's complement.	L2	6M
		OR		
2	a	Convert the following numbers i) (CD)16 = ( )2 ii) (1546)8 = ( )16 iii) (101101.10)2=( )8	L5	6M
	b	Perform the following Using BCD arithmetic $(7129)_{10} + (7711)_{10}$	L5	6M

UNIT-II

3	a	Design the circuit by Using NOR gates F= (X+Y). (X'+Y'+Z')	L5	6M
	b	Simplify the Boolean expression using K-MAP F(A,B,C,D) = ∑m(1,2,3,8,9,10,11,14)+d(7,15)	L5	6M
		OR		
4	a	Explain NAND- NOR implementations.	L2	6M
	b	Simplify the Boolean expression using K-map F(A,B,C,D,E)= ∑m(0,1,4,5,16,17,21,25,29)	L2	6M

UNIT-III

5	a	Explain Carry Look ahead Generator.	L2	6M
	b	Implement the following Boolean function using 8:1 multiplexer F(A, B, C, D) = A'BD' + ACD + A'C' D +B'CD	L5	6M
		OR		
6	a	Design the combinational circuit binary to gray code.	L2	6M
	b	Explain about Binary Half Adder.	L2	6M

UNIT-IV

7	a	Explain the Logic diagram of JK flip-flop.	L2	6M
	b	Design and draw the 3 bit up-down synchronous counter.	L5	6M
		OR		
8	a	Explain about Shift Registers.	L2	6M
	b	Draw and explain the operation of D Flip-Flop.	L5	6M

UNIT-V

9	a	Explain about Error correction & Detection Codes.	L2	6M
	b	Explain about the construction of 4 X 4 RAM.	L2	6M
		OR		
10	a	Explain about Hamming Code with example.	L2	6M
	b	Explain different types of ROM.	L2	6M

*** END ***